Abstract

Developing systems software for new hardware architectures is challenging. Developing low-level embedded system firmware or operating system software while evolving a processor architectures is harder still. narvie is a Read Evaluate Print Loop (REPL) that provides an interactive interface to an open-source RISC-V (RV32I) processor design. narvie allows operating systems researchers and hardware architects to interact with a RISC-V processor implementation running in an iCE40 low-power low-pinctoul FPGA.

Existing instruction REPs

Rappel\(^6\) (linux) and WinRepl\(^4\) (Windows) execute individual x86 instructions on the host computer by inserting instructions into the executable memory of a running child process.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>imm[11:0]</th>
<th>rs1</th>
<th>funct</th>
<th>rd</th>
<th>upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td>addi x1, x1, 0x567</td>
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</table>

Idea

narvie provides a terminal user interface. Once the user enters an RISC-V instruction mnemonic \(^1\), narvie converts the input into a binary instruction \(^2\) and sends it to the FPGA via a serial port \(^3\). Finally, the registers are read back and displayed to the user \(^4\).

narvie exposes the RISC-V instruction set architecture in a very basic form and demonstrate in a concrete way what individual instructions do. By allowing evaluation of individual instructions, narvie will help programmers to gain understanding of RISC-V.

Hardware Implementation

1. Load the instruction from UART.
2. Clock the processor once.
3. Replace the instruction by a no-op.
4. Clock the processor four more times.
5. Send the registers over UART.

The processor clock does not run continuously. The clock starts when an instruction is received and stops as soon as the instruction has been fully evaluated. As narvie uses a processor with a five stage pipeline, five rising edges of the processor clock are required for each instruction.

Lattice mobile development board containing iCE40 FPGAs that can be programmed and communicated with via USB. Source: www.latticesemi.com

Timing diagram showing the five processor clocks that run to evaluate an instruction. The signals Has received instruction and Received instruction are set by hardware listening to UART. Source: wavedrom.com

Contributions:

1. narvie is a acronym for native RISC-V instruction evaluator.
4. zerosum0x0. WinRepl. 2017. URL: https://github.com/zerosum0x0/WinREPL.

References:

1. narvie is a new tool enabling evaluation of individual RISC-V instructions, enable experimentation and exploration.

source: www.semiconductorstore.com